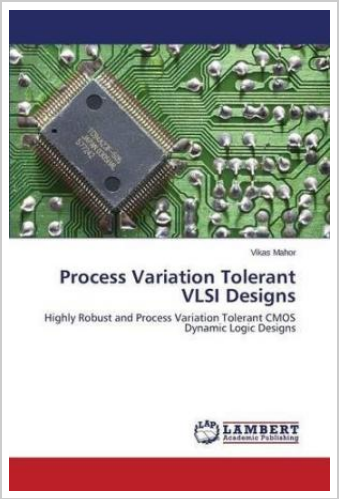

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Process Variation Tolerant VLSI Designs

By Vikas Mahor

LAP Lambert Academic Publishing Jan 2015, 2015. Taschenbuch. Condition: Neu. Neuware - Dynamic gates have been excellent choice in the design of high-performance modules in modern microprocessors. The only limitation of dynamic gates is their relatively low noise margin compared to that of standard CMOS gates. Traditionally, this issue has been resolved by employing a pMOS keeper circuit that compensates for leakage current of the pull-down nMOS network. In the earlier technology nodes, the keeper circuit could improve reliability of the dynamic gates with minor performance penalty. However, aggressive scaling trends of CMOS technology along with increasing levels of process variations have reduced effectiveness of the traditional keeper approach. This problem is more severe in wide fan-in dynamic gates due to the large number of leaky nMOS devices connected to the dynamic node. In this work a process variation tolerant wide fan-in dynamic OR gate with two new keeper designs is proposed which are capable of reducing the contention between the keeper and PDN and hence capable of reducing the power dissipation and delay. 80 pp. Englisch.

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