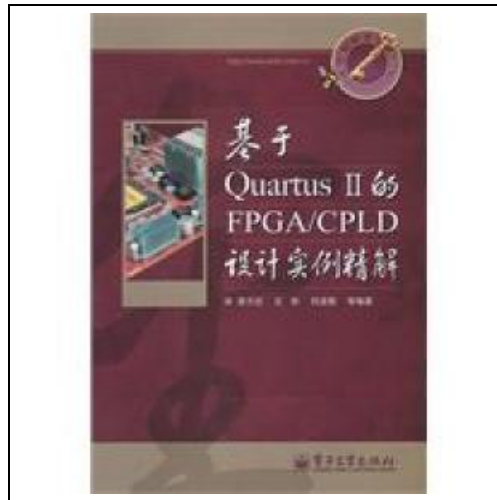# Design based on QUARTUS2 fine solution of FPGAGPLD



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