



Using VLSI to Reduce Serialization and Memory Traffic in Shared Memory Parallel Computers (Classic Reprint) (Paperback)

By Susan Dickey

Forgotten Books, 2018. Paperback. Condition: New. Language: English . Brand New Book ***** Print on Demand *****. Excerpt from Using Vlsi to Reduce Serialization and Memory Traf?c in Shared Memory Parallel Computers Hardware design and assembly of a multiprocessor with a very high degree of parallelism therefore poses no new problems. However, actually using all the processing power that can theoretically be generated presents a two-fold challenge. First, several thousand processors must be coordinated in such a way that their aggregate power is applied to useful computation. Serial procedures in which one processor works while the others wait become bottlenecks that drastically reduce the power obtained. The cost of serial bottlenecks rise linearly with the number of processors involved; in any highly parallel architecture, they must be eliminated. Second, the machine must be programmable by humans. High degrees of parallelism require simple languages and easy-to-use facilities for designing, writing, and debugging parallel programs in order to be effectively used. Our group has proposed [5] that the hardware and software design of a highly parallel computer should meet the following goals. About the Publisher Forgotten Books publishes hundreds of thousands of rare and classic books. Find more at This book is a...



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