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## Performance Evaluation of Parallel Packet-Processing Architectures Using SystemC-based Modeling and Refinement

By Sören Sonntag

Shaker Verlag Feb 2007, 2007. Taschenbuch. Condition: Neu. Neuware - Network nodes, such as broadband access components, are facing new design challenges due to recent trends in applications and technologies. Stringent constraints on platform costs, performance, and power dissipation increasingly require novel programmable application-specific multi-processor architectures to be deployed. Early design space exploration is required to build a proper hardware platform. Multiple processing elements and on-chip interconnects need to be integrated. As complexity grows there is a demand to efficiently evaluate the performance of the complete system. Due to the complexity and heterogeneity it is no longer feasible to start with a model at the register-transfer level. Abstractions must be found to allow performance evaluation even in the concept phase of the design flow. A system-level performance evaluation framework is required to explore multi-processor architectures and to quantitatively evaluate different design alternatives. Due to a lack of these frameworks, today's architectures exhibit overprovisioning of resources instead of configurability in general or reconfigurability at run-time. This leads to systems that are either designed too pessimistically in order to meet all traffic requirements or too optimistically due to inaccurate approximations of resource utilizations caused by non-deterministic real-life workload. Multi-processor architectures can address...



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